COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on November 6, 2009. At the time the Examiner mailed the Office Action claims 1, 3-26, 34, 36, 65 and 66 were pending. By way of the present response the Applicant has: 1) amended claims 4, 12, 22 and 66; 2) not canceled any claims; and, 3) not added any claims. As such, claims 1, 3-26, 34, 36, 65 and 66 remain pending. The Applicant respectfully requests reconsideration of the present application and the allowance of claims 1, 3-26, 34, 36, 65 and 66.

Dependent Claim 66

The Examiner has rejected dependent claim 66 under 35 U.S.C. § 112, second paragraph, as being indefinite. According to the Examiner:

> Claim 66 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant's variable transistor 1118 does not have a second terminal which is only coupled to a source terminal of the switch transistor. When transistor 1116 is on, then the second terminal of the variable transistor will be connected to the drain of 114 and all of the pass gates. Thus, claim 66 is considered misdescriptive. For the purposes of examination, examiner will interpret the limitation of "a second terminal of the variable impedance transistor is coupled to only a source terminal of the switch transistor" as "a second terminal of the variable impedance transistor is coupled to the switch transistor."

The Applicant has herewith amended claim 66 to recite:

> 66. The programmable delay cell of claim 4, wherein a first terminal of a variable impedance transistor is coupled to a high supply rail such that a drain terminal of the switch transistor does not reside between the source terminal of the switch transistor and the variable impedance transistor and a second terminal of the variable impedance transistor is coupled to only a source terminal of the switch transistor.

The Applicant respectfully submits that claim 66 is not indefinite as the location of the source relative to the drain of the variable impedance transistor regarding its coupling to the high supply rail is clearly stated.

Independent Claims 1, 7, 18 and 34

The Examiner has rejected independent claims 1, 7, 18 and 34 under 35 U.S.C. § 103 as being obvious in view of U.S. Patent No. 6,868,504 (hereinafter, "Lin") and U.S. Patent Publication No. 2003/0102894 (hereinafter, "Lo"). Each of claims 1, 7, 18 and 34 recite:

> a capacitor coupled to a low supply rail;
> a conductor coupled to an output of said programmable delay cell; and
> two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor, wherein an impedance of each of said pass gates is to be controlled by a respective control signal.

According to the Examiner:

> Lin teaches in his Figure 3 a programmable delay cell comprising a capacitor coupled to a low supply rail (within 63, on the right); a conductor (wire connected between the input of 45 and 54) coupled to an output of said programmable delay cell (Out); but fails to teach two or more pass gates coupled to said conductor and to said capacitor. However, Lo teaches replacing transistors with pass gates ([0027] and as shown in comparison of Figure 7 with Figure 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention to replace Lin's transistors (47-53) with pass gates "in order to achieve fully rail to rail voltage swings," as taught by Lo (in [0038]).

The Applicant does not understand the Examiner's rejection. The Examiner's rejection explicitly states that the Lin reference discloses a capacitor, a low supply rail and a conductor.

Moreover, the Examiner's rejection further states that Lin "fails to teach two or more pass gates." Thus, a straightforward reading of the Examiner's rejection indicates that the Examiner believes that Lin discloses a capacitor, a low supply rail and a capacitor but does not disclose two or more pass gates.

Therefore, the Examiner's statement that "it would have been obvious…to replace Lin's transistors (47-53) with [Lo's] pass gates" does not contribute to any theory of rejection. The Examiner did not reason that transistors (47-53) of Lin meet any of the Applicant's claim limitations. Therefore their replacement with Lo's pass gates is irrelevant. The Applicant respectfully requests the Examiner to more clearly define a theory of rejection that articulates the replacement of a cited feature which has been used to meet one of the Applicant's claim elements with another cited feature.

Independent Claims 4, 12 and 22

The Examiner has rejected independent claims 4, 12 and 22 under 35 U.S.C § 103 as being obvious in view of Lin and U.S. Patent No. 4,584,492 (hereinafter, "Sharp"). Each of independent claims 4, 12 and 22 recited the following as of the writing of the Examiner's action:

> a conductor coupled to an output of said programmable delay cell;
> a switch transistor coupled to the conductor; and
> a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

According to the Examiner:

> Lin teaches (Figure 3) a conductor (wire connected to a node between the input of 45 and 54) coupled to an output of said programmable delay cell (OUT); but fails to teach a variable impedance transistor. However, Sharp teaches a temperature compensated input buffer (Figure I) comprising a switch transistor (20) and a variable impedance transistor (23) coupled to a high

> supply rail (as shown) and to a source terminal of the switch transistor (as shown and further explained below), wherein an impedance of said variable impedance transistor is to be determined by a control signal (1 8). Sharp teaches in his specification that "the feedback on line 18 compensates for the temperature changes and process variations" (column 4, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time of invention to use Sharp's temperature compensated input buffer in place of Lin's input buffer (44) in order to be maintain functionality over a wide range of temperatures (as explained by the abstract). It is noted that the claim does not require that the variable impedance transistor is coupled directly between the high supply rail and the source terminal of the switch transistor, only that it is coupled to both.

The Applicant has amended each of independent claims 4, 12 and 22 to recite:

> a conductor coupled to an output of said programmable delay cell;
> a switch transistor coupled to the conductor; and
> a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch transistor and the variable impedance transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

The Applicant respectfully submits that the Examiner's creative interpretation of claims 4, 12 and 22 is moot in view of the amendments made to these claims in the present response. Therefore, the Applicant respectfully requests the removal of the Examiner's rejection.

Because the Applicant has shown the patentability of all pending independent claims, the Applicant respectfully requests the removal of all claim rejections and the allowance of the instant application.

CONCLUSION

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Robert B. O'Rourke at (408) 720-8300.

Respectfully submitted,

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